Academic Regulations-M.Tech. 2009-10

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
Academic Regulations For The Award Of Full Time M.Tech. P.G. Degree
(WITH EFFECT FROM THE ACADEMIC YEAR 2009-10)

The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech. Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the University for each programme, from time to time.

Admissions shall be made either on the basis of merit rank obtained by the qualified candidates at an Entrance Test conducted by the University or on the basis of GATE / PGECET score, subject to reservations prescribed by the University or Government policies from time to time.

2.0 **COURSE WORK:**

2.1 A Candidate after securing admission must pursue the M.Tech. course of study for Four semesters duration.
2.2 Each semester shall be of 20 weeks duration including all examinations.
2.3 A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

3.0 ATTENDANCE:

3.1 A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance on cumulative basis of all subjects/courses in the semester.
3.2 Condonation of shortage of attendance up to 10% i.e., from 65% and above and less than 75% may be given by the college on the recommendation of the Principal.
3.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.
3.4 If the candidate does not satisfy the attendance requirement he is detained for want of attendance and shall reregister for that semester. He / she shall not be promoted to the next semester.

4.0. EVALUATION:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

4.1 For the theory subjects 60% of the marks will be for the External End Examination. While 40% of the marks will be for Internal Evaluation, based on the better of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (I-IV units) and another immediately after the completion of instruction (V-VIII) units with Three questions to be answered out of four in 2hours, evaluated* for 40 marks.

*****Note: All the Questions shall be of equal weightage of 10 marks and the marks obtained for 3questions shall be extrapolated to 40 marks, any fraction rounded off to the next higher mark

4.2 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day to day performance.

4.3 For Seminar there will be an internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts at the end of IV semester instruction.

4.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

4.5 In case the candidate does not secure the minimum academic requirement in any of the subjects (as specified in 4.4.) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

5.0 RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL EVALUATION MARKS:

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

5.1 The candidate should have completed the course work and obtained examinations results for I & II semesters.

5.2 He should have passed all the subjects for which the Internal evaluation marks secured are more than 50%.

5.3 Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

5.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

5.5 For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the Registrar, JNTUA payable at Anantapur along with the requisition through the Principal of the respective college.

5.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

6.0 EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ institute.

6.1 Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Sem)

6.2 An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor and one internal senior expert shall monitor the progress of the project work.

6.3 The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest and one calendar year from the date of registration for the project work. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

6.4 The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.

6.5 A candidate shall be allowed to submit the thesis / dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva-voce examination may be conducted once in two months for all the candidates submitted during that period.

6.6 Three copies of the Thesis / Dissertation certified in the prescribed from by the supervisor & HOD shall be presented to the H.OD. One copy is to be forwarded to the University and one copy to be sent to the examiner.

6.7 The college shall submit a panel of three experts for a maximum of 5 students at a time. However, the thesis / dissertation will be adjudicated by one examiner nominated by the University.

6.8 If the report of the examiner is favorable viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis / dissertation. The board shall jointly report candidates work as:

1.	Very Good	Grade A
2.	Good	Grade B
3.	Satisfactory	Grade C
4.	Not satisfactory	Grade D

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

7.0 AWARD OF DEGREE AND CLASS:

A candidate shall be eligible for the award of respective degree if he satisfies the minimum academic requirements in every subject and secures 'satisfactory' or higher grade report on his thesis/dissertation and viva-voce. Based on overall percentage of marks obtained, the following class is awarded.

First class with Distinction:	70% or more
First class	below 70% but not less than 60%
Second class	below 60% but not less than 50%

8.0 WITH – HOLDING OF RESULTS:

If the candidate has not paid dues to the university or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed/ promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to 4.5 and 2.3 sections. Whereas they continue to be in the academic regulations they were first admitted.

10.0 GENERAL:

i. **The academic regulations should be read as a whole for purpose of any interpretation**.
ii. **Disciplinary action for Malpractice / improper conduct in examinations is appended**.
iii. **There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.**
iv. **Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".**
v. **In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.**
vi. **The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.**

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RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
6.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.

7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
8.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions : (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, ANANTAPUR

Course Structure and Syllabi for M.Tech.

VLSI SYSTEM DESIGN VLSI SYSTEMS AND VLSI

for affiliated Engineering Colleges2009-10

I YEAR I SEMESTER

S. No	Course code	Subject	Theory	Lab.	Credits
1.	9D57101	VLSI Technology	4		4
2.	9D57102	Analog IC Design	4		4
3.	9D57103	Digital IC Design	4		4
4.	9D57104	Hardware Description Languages	4		4
5.	9D57105	Hardware Software Co-design	4		4
6.	9D57106a 9D57106b 9D57106c	**ELECTIVE I** a. Embedded system Concepts b. System Modeling & Simulation c. ASIC Design	4		4
7.	9D57107	Digital IC Design Lab		3	2
		contact periods/week	24	3	26
			Total 27		

I YEAR II SEMESTER

S. No	Course code	Subject	Theory	Lab.	Credits
1.	9D55201	Testing & Testability	4		4
2.	9D57202	Low Power VLSI Design	4		4
3.	9D57203	Algorithms for VLSI Design Automation	4		4
4.	9D55204	FPGA Architectures & Applications	4		4
5.	9D57205	Scripting Language for VLSI Design Automation	4		4
6.	9D57206a 9D57206b 9D57206c	**ELECTIVE II** a. Nano Electronics b. Cryptography & Network Security c. Real Time Operating Systems	4		4
7.	9D57207	Mixed Signal Lab		3	2
		contact periods/week	24	3	26
			Total 27		

II YEAR (III & IV Semesters)

S. No	Course code	Subject		credits
1	9D57401	Seminar		2
2	9D57402	Project work		16

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M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57101) VLSI TECHNOLOGY

UNIT I: REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

UNIT II: BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT III: LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

UNIT IV: LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNITV: COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT VI: SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VII:FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT VIII: INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

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M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57102) ANALOG IC DESIGN

UNIT I: MOS transistors- modeling in linear, saturation and cutoff high frequency equivalent circuit.

UNIT II & III: INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT IV: OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded–Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator . Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.

UNIT V: SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

UNIT VI: SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-II: Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.

UNIT VII: DATA CONVERTERS: Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating ,Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT VIII: OVER SAMPLING CONVERTERS AND FILTERS: Over Sampling With and Without Noise Shaping .Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

TEXT BOOKS:

1. D.A.JOHN & KEN MARTIN: "Analog Integrated Circuit Design". John Wiley, 1997.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuit" Tata-Mc GrawHill, 2002

REFERENCES:

1. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002
2. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57103) DIGITAL IC DESIGN

UNIT I: CMOS inverters -static and dynamic characteristics.

UNIT II: Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT III: Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design.

UNIT IV: Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT V: Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

UNIT VI&VII: LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT VIII:SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999
2. Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1997
3. Eugene D Fabricus, "Introduction to VLSI Design,"McGraw Hill International Edition.1990

REFERENCES:

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000
2. Neil H E West and Kamran Eshranghian,"Principles of CMOS VLSI Design: A System Perspective", Addision-Wesley 2nd Edition,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation". New York: IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, "Analysis and Design of Digital Integrated Circuits", Third Edition, McGraw-Hill, 2004.

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M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57104) HARDWARE DESCRIPTION LANGUAGES

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT V

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT VI

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT VII

INTRODUCTION TO VHDL: An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

UNIT VIII

BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

TEXT BOOKS:

1. M.D.CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Z.NAWABI, "VHDL Analysis and Modeling of Digital Systems", (2/E), McGraw Hill, 1998.

REFERENCES:

1. M.G.ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.
2. PERRY, "VHDL", (3/E), McGraw Hill.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57105) HARDWARE SOFTWARE CO- DESIGN

UNIT I: CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

UNIT II: CO- SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

UNIT III: PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT IV: TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT V: COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT VI: DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT VII: LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages,

UNIT VIII: LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, kluwer academic publishers

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M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

ELECTIVE I
(9D57106a) EMBEDDED SYSTEM CONCEPTS

UNIT I : AN INTRODUCTION TO EMBEDDED SYSTEMS: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

UNIT II: PROCESSOR AND MEMORY ORGANIZATION: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT III: DEVICES AND BUSES FOR DEVICE NETWORKS: I/O Devices, Timer and Counting Devices, Serial Communication Using The "I^2C" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

UNIT IV : DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM: Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT V: INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VI : PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++, VC++ AND JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT VII: HARDWARE–SOFTWARE CO-DESIGN IN AN EMBEDDED SYSTEM: Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process,

UNIT VIII: DESIGN CYCLE IN THE DEVELOPMENT PHASE FOR AN EMBEDDED SYSTEM, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

TEXTBOOKS:

1. Rajkamal, "Embedded systems: Architecture, Programming and Design" TMH.
2. wayne wolf, "Computers as a component: principles of embedded computing system design".

REFERENCES:

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded systems design:Real world design be Steve Heath; Butterworth Heinenann, Newton mass USA 2002
4. Data communication by Hayt.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEMESTER (VLSI SYSTEM DESIGN)	**Th**	**C**
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ELECTIVE I

(9D57106b) SYSTEM MODELLING & SIMULATION

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS: Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT V

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

UNIT VI

MARKOV PROCESS: Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT VII

EVENT DRIVEN MODELS: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

UNIT VIII

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1. System Modeling & Simulation, an Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCES:

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

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M.Tech. I SEMESTER (VLSI SYSTEM DESIGN)	**Th**	**C**
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ELECTIVE I

(9D57106c) ASIC DESIGN

UNIT I: ASIC DESIGN STYLES: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

UNIT II: ASICS – PROGRAMMABLE LOGIC DEVICES: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Intoduction, selected families – design outline.

UNIT III: ASICS –DESIGN ISSUES: Design methodologies and design tools – design for testability – economies.

UNIT IV: ACISS CHARACTERISTICS AND PERFORMANCE: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT V: ASICS-DESIGN TECHNIQUES: Overview- Design flow and methodology-Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

UNIT VI: LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation.

UNIT VII: ASIC CONSTRUCTION: Floor planning, placement and routing system partition.

UNIT VIII: FPGA PARTITIONING: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

TEXT BOOKS:

1. L.J.Herbst,"Integrated circuit engineering", OXFORD SCIENCE Publications, 1996.

REFERENCES:

1. M.J.S.Smith, "Application - Specific integrated circuits", Addison-Wesley Longman Inc 1997.

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M.Tech. I SEMESTER (VLSI SYSTEM DESIGN) **L** **C**
3 **2**

(9D57107) DIGITAL IC DESIGN LAB

Experiments devised on the following

1. Digital Circuits Description using Verilog and VHDL.
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

NOTE: Required Software Tools:

1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D55201) TESTING & TESTABILITY

UNIT I: INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II: FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT III: TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT IV&V: DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT VI: BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT VII: MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

UNIT VIII: BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.

REFERENCES:

1. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
2. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57202) LOW POWER VLSI DESIGN

UNIT I: LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II: MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV: DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V: CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI: LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII: LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII: SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1. Yeo Rofail/ Gohl(3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia 1st Indian reprint,2002.
2. Gary K. Yeap,"Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCES:

1. Douglas A.Pucknell & Kamran Eshraghian, "Basic VLSI Design", 3rd edition PHI.
2. J.Rabaey, "Digital Integrated circuits", PH,1996
3. Sung-mo Kang and yusuf leblebici, "CMOS Digital ICs", 3rd edition TMH 2003 .
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D57203) ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT I : PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II: GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III: Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV: MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V: LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI: HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VII: PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VIII: PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" ,3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI, Hill & Peterson, Wiley, 1993.
2. Modern VLSI Design Systems on silicon – Wayne Wolf, Pearson Edn Asia, 2/e, 1998.

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

(9D55204) FPGA ARCHITECTURE & APPLICATIONS

UNIT I: PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II: FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT III: CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT IV: FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT V: REALIZATION OF STATE MACHINE: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT VI& VII: FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT VIII

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS/ REFERENCES:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Pub,1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pub, 1992.

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN)	**Th**	**C**
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(9D57205) SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

UNIT I: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT II&III: PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT IV&V: Inter process Communication Threads, Compilation & Line Interfacing.

UNIT VI&VII: Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT VIII: Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

TEXT BOOKS:

1. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", Oreilly Publications, 3rd Edn., 2000.
3. Tom Christiansen, Nathan Torkington, "PERL Cookbook", Oreilly Publications, 3rd Edn,2000

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

ELECTIVE II
(9D57206a) NANO ELECTRONICS

UNIT I:
TECHNOLOGY AND ANALYSIS: Film Deposition Methods, Lithography, Material Removing Technologies, Etching and Chemical, Mechanical Processing, Scanning Probe Techniques.

UNIT II:
CARBON NANO STRUCTURES: Carbon Clusters, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT III:
LOGIC DEVICES: Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT IV:
RADOM ACESS MEMORIES: High Permitivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT V&VI:
MASS STORAGE DEVICES:
Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT VII&VIII:
DATA TRANSIMISSION, INTERFACES AND DISPLAYS:
Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:
1. Rainer Waser, "Nano Electronics and Information Technology", Wiley VCH, April 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Interscience, May 2003

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

ELECTIVE II
(9D57206b) CRYPTOGRAPHY & NETWORK SECURITY

UNIT I: SYMMETRIC CIPHERS: Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

UNIT II: PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS: Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT III: NETWORK SECURITY PRACTICE: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT IV: SYSTEM SECURITY: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

UNIT V: WIRELESS SECURITY: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT VI: SECURE NETWORKING THREATS: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT VII: ENCRYPTION TECHNIQUES: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT VIII: DESIGNING SECURE NETWORKS: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security – Principles And Practices", Pearson Education, 3rd Edition, 2003.
2. Sean Convery, " Network Security Architectures, Published by Cisco Press, 1/e. 2004.

REFERENCES:

1. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
2. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
3. Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.
4. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", 3rd Edition, Pearson Education, 2003.
5. Jeff Crume, "Inside Internet Security" Addison Wesley, 2005.

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **Th 4** **C 4**

ELECTIVE II

(9D57206c) REAL TIME OPERATING SYSTEMS

UNIT I: INTRODUCTION TO UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT II&III: REAL TIME SYSTEMS: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT IV: APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

UNIT V: OPERATING SYSTEMS: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT VI: FAULT TOLERANCE TECHNIQUES: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

UNIT VII: CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT VIII: RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

1. Richard Stevens, "Advanced Unix Programming".
2. Jane W.S. Liu, "Real Time Systems", Pearson Education.
3. C.M.Krishna, KANG G. Shin, "Real Time Systems", McGraw.Hill

REFERENCES:

1. VxWorks Programmers Guide
2. www.tidp.org
3. www.kernel.org
4. http://www.xml.com/ldd/chapter/book

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M.Tech. II SEMESTER (VLSI SYSTEM DESIGN) **L** **C**

3 **2**

(9D57207) MIXED SIGNAL LABORATORY

Experiments devised on the following

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

NOTE: Required Software Tools:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. IV SEMESTER (VLSI SYSTEM DESIGN) **C**
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(9D57401) SEMINAR

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. IV SEMESTER (VLSI SYSTEM DESIGN) **C**
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(9D57402) PROJECT WORK

The Project Work should be on a contemporary topic relevant to the core subjects of the course. It should be original work of the candidate.

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